Electronic Version
Stylesheet Version v1.1.1

[STACK CHIP PACKAGE STRUCTURE]

Abstract

A stack chip package structure is provided. One principal feature of the structure is the formation of a few peripheral surfaces (e.g. ladder or lead-angle surfaces) at the bottom peripheral sections of a stack structure. When the stack structure is attached to a surface of a die through an adhesive layer, the thickness of the adhesive layer under a peripheral section of the stack structure is greater than a central region. Therefore, as the chip package is subjected to a thermal stress test, the adhesive layer under the peripheral sections of the stack structure is able to provide some buffering against thermal stress so that the stress concentration around the stack structure is reduced. Consequently, damages of the die surface due to stress are prevented and the average working life of the chip package is extended.